WHAT IS CLAIMED IS:

1. A semiconductor device having a multiple layered ridge, the semiconductor device comprising:

an electrode layer that covers at least an upper face of the ridge and at least one side face of the ridge in a longitudinal direction, wherein thickness of said electrode layer on the upper face and the thickness of said electrode layer on the at least one side face of the ridge are substantially same.

2. The semiconductor device according to Claim 1, wherein the thickness of said electrode layer on said at least one side face of said ridge is not smaller than 150 nm.

3. The semiconductor device according to Claim 2, wherein the ridge is supported by a substrate having a top surface and a bottom surface, wherein the ridge is formed at the top surface of the ridge at a first region of the top surface, wherein the top surface of the substrate has a second region located to at least one side of the ridge, and wherein said electrode layer further covers the second region with a thickness that is not smaller than 150 nm.

4. A method of manufacturing a semiconductor device having a multiple layered ridge, the method comprising the steps of:

(a) sequentially forming the multiple layers of the ridge; and

(b) forming an electrode layer which covers at least an upper face of the ridge and at least one side face of the ridge in the longitudinal direction in such a manner that the thickness of the electrode layer on the upper face and the thickness of the electrode layer on the at least one side face of the ridge are substantially the same.

5. The method according to Claim 4, wherein the thickness of said electrode layer on the at least one side face of the ridge is not smaller than 150 nm.

6. The method according to Claim 5, wherein the ridge is supported by a substrate having a top surface and a bottom surface, wherein the ridge is formed at the

top surface of the ridge at a first region of the top surface, wherein the top surface of the substrate has a second region located to at least one side of the ridge, and wherein the electrode layer further covers the second region with a thickness that is not smaller than 150 nm.

7. The method according to Claim 4, wherein when forming the electrode layer, an electrode forming material is supplied to the at least one side face of the ridge from the upper side.

8. The method according to Claim 4, wherein the ridge is formed at a surface of a substrate, wherein the substrate has a normal vector perpendicular to the surface of the substrate's first surface, wherein step (b) comprises the steps of:

(c) exposing the ridge and the substrate to a material deposition process which emits material from a source to the ridge and substrate along a deposition axis with the normal vector of the substrate being inclined at an angle of greater than zero degrees from the deposition direction;

(d) during the performance of step (c), rotating the ridge about the normal vector of the substrate.

9. A semiconductor device comprising:

a substrate having a first surface and a second surface;

a ridge formed at the first surface of the substrate and comprising at least one layer of a semiconductor material, the ridge having an upper face and at least two side faces; and

a conductive layer disposed on at least a portion of the ridge such that the conductive layer covers at least one side face of the ridge with a first thickness (T_1) at said portion, and further covers the ridge's upper face with a second thickness (T_2) at said portion, wherein the first thickness is equal to or greater than fifty percent of the second thickness.

10. The semiconductor device according to Claim 9, wherein the conductive layer comprises one or more sublayers, each sublayer comprising a

material which has less than 5% of gold by weight.

11. The semiconductor device according to Claim 9, wherein the conductive layer comprises one or more sublayers, each sublayer comprising a material which has hardness equal to or greater than 30 on the Vickers scale when the material is in its bulk crystalline state.

12. The semiconductor device according to Claim 9, wherein the conductive layer comprises one or more sublayers, each sublayer comprising a material which has a ductility when the material is in its bulk crystalline state which is lower than the ductility of gold.

13. The semiconductor device according to Claim 9, wherein the conductive layer comprises one or more sublayers, each sublayer having a lustrous surface morphology.

14. The semiconductor device according to Claim 9, wherein the ridge is formed on top of the first surface of the substrate.

15. The semiconductor device according to Claim 9, wherein the ridge is formed in the first surface of the substrate with one or more grooves formed in the substrate to define the two or more sides of the ridge.

16. The semiconductor device according to Claim 9, wherein the ridge further comprising a dielectric layer disposed on at least said portion of the ridge and located between the at least one side face of the ridge and the conductive layer.

17. The semiconductor device according to Claim 9, wherein said first thickness is greater than or equal to 150 nm.

18. The semiconductor device according to Claim 9, wherein said first thickness is less than or equal to one-hundred and twenty percent of the second

thickness.

19. The semiconductor device according to Claim 9, wherein the first thickness is equal to or greater than sixty percent of the second thickness.

20. The semiconductor device according to Claim 19, wherein the first thickness is less than or equal to said second thickness.

21. The semiconductor device according to Claim 9, wherein said first thickness is substantially equal to said second thickness.

22. A semiconductor device comprising:

a substrate having a first surface and a second surface;

a ridge formed at the first surface of the substrate and comprising at least one layer of a semiconductor material, the ridge having an upper face and at least two side faces; and

a conductive layer disposed on at least a portion of the ridge such that the layer covers at least one side face of the ridge with a first thickness (T_1) at said portion, and further covers the ridge's upper face with a second thickness (T_2) at said portion, wherein said first thickness is greater than or equal to 150 nm.

23. The semiconductor device according to Claim 22, wherein the ridge is formed on top of the first surface of the substrate.

24. The semiconductor device according to Claim 22, wherein the ridge is formed in the first surface of the substrate with one or more grooves formed in the substrate to define the two or more sides of the ridge.

25. The semiconductor device according to Claim 22, wherein the ridge further comprising a dielectric layer disposed on at least said portion of the ridge and located between the at least one side face of the ridge and the conductive layer.

26. The semiconductor device according to Claim 22, wherein said first thickness is greater than or equal to fifty percent of the second thickness and less than or equal to one-hundred and twenty percent of the second thickness.

27. The semiconductor device according to Claim 22, wherein the first thickness is equal to or greater than sixty percent of the second thickness.

28. The semiconductor device according to Claim 27, wherein the first thickness is less than or equal to said second thickness.

29. The semiconductor device according to Claim 22, wherein said first thickness is substantially equal to said second thickness.

30. The semiconductor device according to Claim 22, wherein said first thickness is greater than or equal to 200 nm.

31. The semiconductor device according to Claim 22, wherein the conductive layer material comprises one or more sublayers, each sublayer comprising a material which has less than 5% of gold by weight.

32. The semiconductor device according to Claim 22, wherein the conductive layer comprises one or more sublayers, each sublayer comprising a material which has hardness equal to or greater than 30 on the Vickers scale when the material is in its bulk crystalline state.

33. The semiconductor device according to Claim 22, wherein the conductive layer comprises one or more sublayers, each sublayer comprising a material which has a ductility when the material is in its bulk crystalline state which is lower than the ductility of gold.

34. The semiconductor device according to Claim 22, wherein the conductive layer comprises one or more sublayers, each sublayer having a lustrous

surface morphology.

35. A method of manufacturing a semiconductor device having a multiple layered ridge, the method comprising the steps of:

(a) forming a ridge at a first surface of a substrate, the ridge comprising at least one layer of a semiconductor material, and having an upper face and at least two side faces; and

(b) forming a conductive layer by dry deposition on at least a portion of the ridge such that the layer covers at least one of the ridge's side face with a first thickness (T_1) at said portion, and further covers the ridge's upper face with a second thickness (T_2) at said portion, wherein the first thickness is equal to or greater than fifty percent of the second thickness, and wherein the conductive layer covers at least a portion of the at least one semiconductor layer.

36. The method of Claim 35 further comprising the steps of:

forming a patterned mask on the first surface of the substrate prior to the performance of step (b);

stripping the patterned mask with liquid solvent after the performance of step (b) and with the liquid solvent contacting at least a portion of the conductive layer.

37. The semiconductor device according to Claim 35, wherein step (a) comprises the step of forming a dielectric layer on at least said portion of the ridge and located between the at least one side face of the ridge and the conductive layer.

38. The semiconductor device according to Claim 35, wherein the first thickness is greater than or equal to 150 nm.

39. The semiconductor device according to Claim 35, wherein the first thickness is greater than or equal to 200 nm.

40. The semiconductor device according to Claim 35, wherein the first thickness is equal to or greater than fifty percent of the second thickness and is less than or equal to one-hundred and twenty percent of the second thickness.

41. The semiconductor device according to Claim 40, wherein the first thickness is equal to or greater than sixty percent of the second thickness.

42. The semiconductor device according to Claim 41, wherein the first thickness is less than or equal to the second thickness.

43. The semiconductor device according to Claim 35, wherein the first thickness is substantially equal to the second thickness.

44. The method according to Claim 35, wherein the substrate has a normal vector perpendicular to the surface of the substrate's first surface, wherein step (b) comprises the steps of:

(c) exposing the ridge and the substrate to a material deposition process which emits material from a source to the ridge and substrate along a deposition axis with the normal vector of the substrate being inclined at an angle of greater than zero degrees from the deposition direction;

(d) during the performance of step (c), rotating the ridge about the normal vector of the substrate.

45. A method of manufacturing a semiconductor device having a multiple layered ridge, the method comprising the steps of:

(a) forming a ridge at a first surface of a substrate, the ridge comprising at least one layer of a semiconductor material, and having an upper face and at least two side faces; and

(b) forming a conductive layer by dry deposition on at least a portion of the ridge such that the conductive layer covers at least one the ridge's side face with a first thickness (T_1) at said portion, and fu, wherein the first thickness is greater than or equal to 150 nm, and wherrther covers the ridge's upper face with a second thickness

(T_2) at said portionein the conductive layer covers at least a portion of the at least one semiconductor layer.

46. The method of Claim 45 further comprising the steps of:

forming a patterned mask on the first surface of the substrate prior to the performance of step (b);

stripping the patterned mask with liquid solvent after the performance of step (b) and with the liquid solvent contacting at least a portion of the conductive layer.

47. The semiconductor device according to Claim 45, wherein step (a) comprises the step of forming a dielectric layer on at least said portion of the ridge and located between the at least one side face of the ridge and the conductive layer.

48. The semiconductor device according to Claim 45, wherein the first thickness is greater than or equal to 200 nm.

49. The semiconductor device according to Claim 45, wherein the first thickness is equal to or greater than fifty percent of the second thickness and is less than or equal to one-hundred and twenty percent of the second thickness.

50. The method according to Claim 45, wherein the substrate has a normal vector perpendicular to the surface of the substrate's first surface, wherein step (b) comprises the steps of:

(c) exposing the ridge and the substrate to a material deposition process which emits material from a source to the ridge and substrate along a deposition axis with the normal vector of the substrate being inclined at an angle of greater than zero degrees from the deposition direction;

(d) during the performance of step (c), rotating the ridge about the normal vector of the substrate.

51. A semiconductor device comprising:

a substrate having a top surface and a bottom surface;

a ridge formed at the top surface of the substrate and comprising at least one layer of a semiconductor material, the ridge having a base attached to the substrate, an upper face located above the base, a first body section located between the base and the upper face, a second body section located between the first body section and the upper face, and at least a first side face located between the ridge's upper face and the base and located to one side of the first and second body sections, the first side face having a first area which spans over the first body section and a second area which spans over the second body section, the first side face further having a straight mesa slope or a forward mesa slope in the first area and a reverse mesa slope in the second area; and

a dielectric layer disposed on the first side face and covering the first area and at least a portion of the second area which is closest to the first area.

52. The semiconductor device of Claim 51 wherein the dielectric layer is disposed to cover the entire first and second areas.

53. The semiconductor device of Claim 51 wherein the top surface portion of the ridge comprises a material which is more resistance to plasma etching than the material of the dielectric layer.

54. The semiconductor device of Claim 51 further comprising a layer of conductive material disposed over the dielectric layer, the upper face of the ridge, and a portion of the second area of the first side face which is closest to the upper face of the ridge.

55. The semiconductor device of Claim 51 wherein the ridge has a base width (A3) along the cross-sectional width of the base, the base width having a value in a range of 2.7 μm to 4.5 μm;

wherein the ridge has a top width (A1) along the cross-sectional width of the ridge's top face, the top width having a value in the range of forty percent of the

base width to sixty-five percent of the base width;

wherein the ridge has an interface plane between the first and second body sections of the ridge, wherein the ridge has a neck width (A2) along the cross-sectional width of the ridge at the interface plane, and wherein the neck width has a value in the range of eighty percent of the ridge top width to ninety-five percent of the ridge top width.

56. The semiconductor device of Claim 55 wherein the ridge has a first height (H1) from the base to the interface plane and a second height (H2) from the interface plane to the top surface of the ridge, wherein the first height has a value in the range of 1.3 μm to 1.4 μm, and wherein the second height has a value in the range of 0.4 μm to 0.6 μm.

57. The semiconductor device of Claim 51 further comprising a conductive layer disposed over a portion of the first side face at a first thickness (T_1) and an adjacent portion of the upper face of the ridge at a second thickness (T_2), said first thickness being equal to or greater than fifty percent of the second thickness, said conductive layer comprises one or more sublayers, each sublayer comprising a material which has less than 5% of gold by weight.

58. The semiconductor device of Claim 57 wherein said first thickness is greater than or equal to 150 nm.

59. The semiconductor device of Claim 57 wherein the first thickness is less than or equal to one-hundred and twenty percent of the second thickness.

60. The semiconductor device according to Claim 57, wherein the first thickness is equal to or greater than sixty percent of the second thickness.

61. The semiconductor device according to Claim 60, wherein the first thickness is less than or equal to said second thickness.

62. The semiconductor device according to Claim 57, wherein said first thickness is substantially equal to said second thickness.

63. The semiconductor device of Claim 51 further comprising a conductive layer disposed over a portion of the first side face at a first thickness (T_1) and an adjacent portion of the upper face of the ridge at a second thickness (T_2), said first thickness is greater than or equal to 150 nm, said conductive layer comprises one or more sublayers, each sublayer comprising a material which has less than 5% of gold by weight.